

20.1. Treat the Sensor as an Electrical Source

Translate a physical transducer datasheet into an electrical source model before choosing an amplifier topology.

Start with the source

A sensor may look like a Thevenin voltage source, Norton current source, variable resistance, variable capacitance, charge source, bridge, or current loop. That source type determines the first useful analog block.

Datasheet quantities

Extract sensitivity, nominal output, source impedance, excitation, common-mode voltage, bandwidth, offset, drift, nonlinearity, noise and maximum ratings. Keep the conditions attached to every number.

Interface specification

Convert the sensor range into minimum/maximum electrical output, then define allowable loading, required gain, bandwidth, noise, protection and final ADC/output range.

Sensor	Useful electrical model
Strain/pressure bridge	small differential V + common mode
Photodiode	current source junction C
Thermistor/RTD	R(T) requiring excitation
Piezo	charge/voltage source + C
4-20 mA	current source with compliance

Key equations

$$\Delta V_S = S_x \Delta x$$

$$V_{S, \max} = V_0 + S_x x_{\max}$$

$$V_{S, \min} = V_0 + S_x x_{\min}$$

$$A_v \lesssim \frac{V_{OUT, span}}{V_{S, span}}$$

Worked example - translate the physical range first

Use the bridge example developed later in this chapter: VEX = 5 V, gauge factor GF = 2 and full-scale strain of +/-500 microstrain. Translate the physical range into electrical span before choosing gain.

$$\frac{\Delta R}{R} = 2(500 \times 10^{-6}) = 1.0 \times 10^{-3}$$

$$|V_{BRIDGE}| \approx \frac{5}{4}(10^{-3}) = 1.25 \text{ mV}$$

$$V_{S, span} \approx 2(1.25) = 2.50 \text{ mV}$$

$$A \approx \frac{2.0 \text{ V}}{2.50 \text{ mV}} \approx 800$$

The chapter later uses gain about 804 and a 1.65 V midpoint. The important sequence is physical range -> sensor electrical range -> allowed loading/common mode -> gain and ADC range.

Page takeaway

Do not begin with an op amp. Begin by deciding what electrical source the transducer actually presents.

20.2. Resistive Sensors and Wheatstone Bridges

Use bridge excitation and differential measurement to turn tiny resistance changes into measurable voltage while rejecting supply/common-mode terms.

Bridge sensitivity

For a balanced quarter bridge and small fractional resistance change, the output is approximately $V_{EX}/4$ times dR/R . For a strain gauge, $dR/R = GF \cdot \text{strain}$.

Common mode

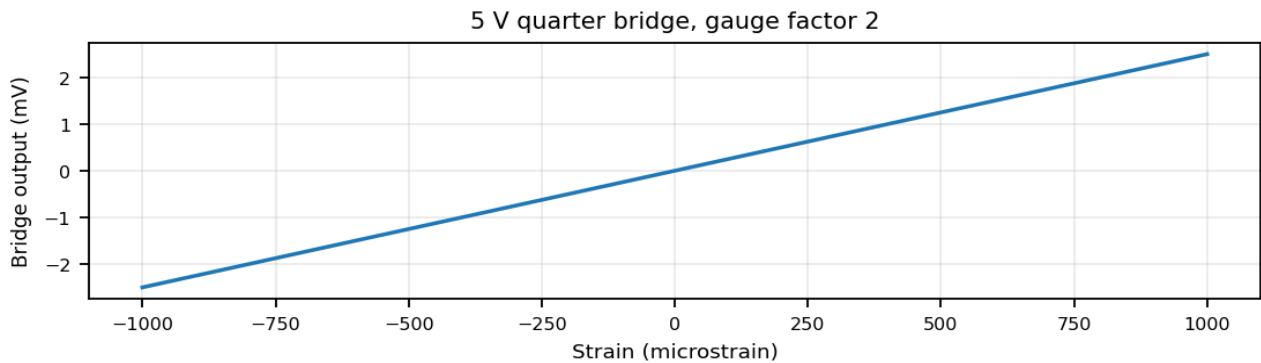
Both bridge midpoint voltages sit near $V_{EX}/2$. The amplifier must tolerate this common-mode voltage while resolving a millivolt-level difference.

Error sources

Excitation accuracy, lead resistance, resistor/gauge mismatch, temperature coefficient and amplifier CMRR all matter. Ratiometric ADC measurement can remove first-order excitation error.

Key equations

$$\begin{aligned}\frac{\Delta R}{R} &= GF \varepsilon \\ V_{BRIDGE} &\approx \frac{V_{EX} \Delta R}{4 R} \\ V_{CM} &\approx \frac{V_{EX}}{2}\end{aligned}$$



Worked example - 350 Ohm quarter bridge at 500 microstrain

The supplied Topic 02 project uses a 350 Ohm active gauge, $GF = 2$, strain = 500 microstrain and $V_{EX} = 5$ V.

$$\frac{\Delta R}{R} = GF \varepsilon = 2(500 \times 10^{-6}) = 0.001$$

$$\Delta R = (350 \, \Omega)(0.001) = 0.35 \, \Omega$$

$$|V_{BRIDGE}| \approx \frac{5}{4}(0.001) = 1.25 \, \text{mV}$$

$$V_{CM} \approx \frac{5}{2} = 2.5 \, \text{V}$$

The amplifier must resolve about 1.25 mV while both bridge nodes sit near 2.5 V common mode. Swapping the active arm or sense nodes reverses output polarity.

RFspice verification

Download [spice/ACDSPICE_Ch20_Topic02_SPICE.zip](#). A 350 Ohm quarter bridge with a 0.35 Ohm active-gauge change demonstrates the millivolt differential signal.

Page takeaway

Bridge design is mainly about extracting a tiny differential change from a much larger common-mode voltage without loading or drift error.

20.3. Thermistors, RTDs and Resistive Sensor Bias

Choose excitation so a resistance sensor produces useful voltage without excessive self-heating, then linearise only as much as the accuracy target requires.

Divider bias

A thermistor plus a fixed resistor converts $R(T)$ to voltage. The fixed resistor near the sensor resistance in the centre of the operating range gives good sensitivity over a limited span.

Self-heating

Sensor current causes I^2R dissipation. The datasheet dissipation constant and thermal time constant determine how much temperature error the electrical measurement itself creates.

Linearisation

Use the full datasheet R - T table, Beta equation, or Steinhart-Hart coefficients in software. Analog parallel/series resistors can flatten a limited range when the system needs a near-linear voltage before conversion.

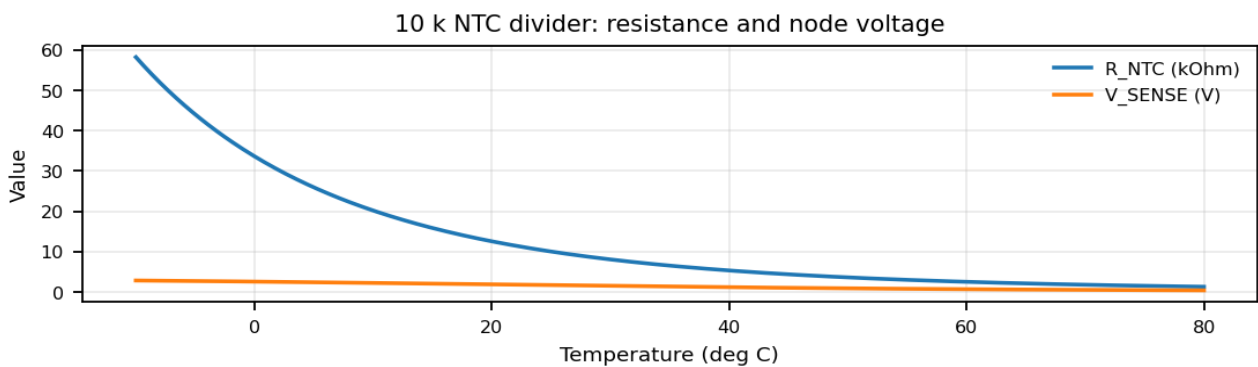
Key equations

$$R(T) = R_0 \exp \left[B \left(\frac{1}{T} - \frac{1}{T_0} \right) \right]$$

$$V_S = V_{EX} \frac{R_T}{R_{FIXED} + R_T}$$

$$I_S = \frac{V_{EX}}{R_{FIXED} + R_T}$$

$$P_{SENSOR} = \frac{V_{EX}^2 R_T}{(R_{FIXED} + R_T)^2}$$



Worked example - 10 kOhm NTC divider from 3.3 V

The Topic 03 project uses a 10 kOhm fixed resistor and representative NTC values 33.6 kOhm at 0 C, 10 kOhm at 25 C and 3.59 kOhm at 50 C.

$$V_S(0^\circ \text{C}) = 3.3 \frac{33.6}{10 + 33.6} = 2.54 \text{ V}$$

$$V_S(25^\circ \text{C}) = 3.3 \frac{10}{10 + 10} = 1.65 \text{ V}$$

$$V_S(50^\circ \text{C}) = 3.3 \frac{3.59}{10 + 3.59} = 0.87 \text{ V}$$

$$P_{NTC, 25C} = \frac{3.3^2 (10 \text{ k}\Omega)}{(20 \text{ k}\Omega)^2} = 0.272 \text{ mW}$$

The divider provides useful voltage sensitivity, but the same current creates sensor self-heating. Replace the representative resistance steps with the chosen thermistor datasheet table or model for hardware design.

RFspice verification

Download [spice/ACDSPICE_Ch20_Topic03_SPICE.zip](#). Step representative NTC resistance values and observe the 3.3 V divider output.

Page takeaway

Bias current is part of the measurement: it creates the signal but can also heat the sensor and create error.

20.4. Photodiodes and Transimpedance Amplifiers

Design directly from detector current and capacitance rather than forcing a current-output sensor through a large resistor.

Transimpedance

With the photodiode at the inverting node, negative feedback holds the detector near constant voltage and converts current to V_{OUT} approximately $-I_{PH}R_F$.

Bandwidth and stability

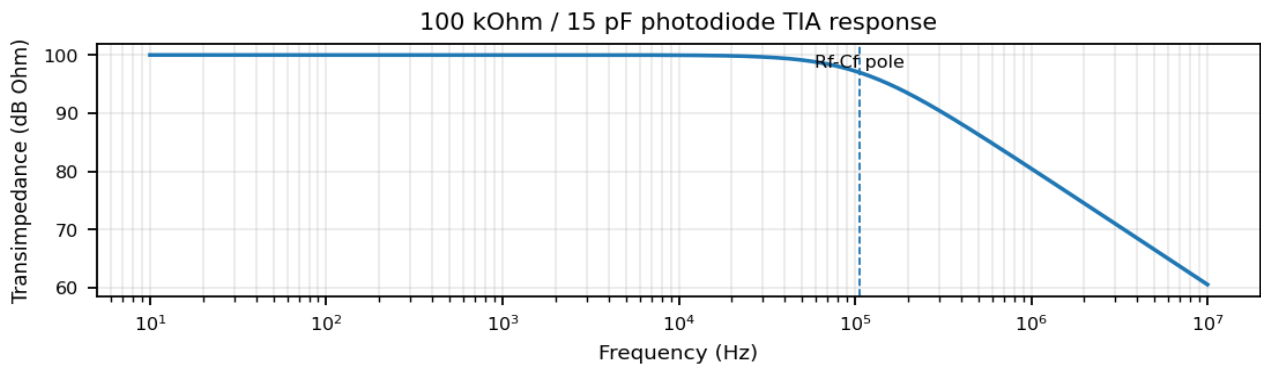
Photodiode junction capacitance, op-amp input capacitance and R_F create noise gain and phase shift. C_F across R_F limits bandwidth but can restore phase margin.

Datasheet use

Use responsivity A/W , dark current, junction capacitance versus reverse bias, shunt resistance and noise-current data. Op-amp selection depends on input current noise, voltage noise, GBW and bias current.

Key equations

$$\begin{aligned} V_{OUT} &\approx -I_{PH}R_F \\ Z_T(0) &\approx -R_F \\ f_{RF-CF} &\approx \frac{1}{2\pi R_F C_F} \end{aligned}$$



Worked example - 100 kOhm / 15 pF photodiode TIA

The Topic 04 project uses $R_F = 100 \text{ k}\Omega$, $C_F = 15 \text{ pF}$ and demonstrates a $1 \text{ }\mu\text{A}$ AC photocurrent.

$$|V_{OUT}| \approx (1 \text{ }\mu\text{A})(100 \text{ k}\Omega) = 0.10 \text{ V}$$

$$|Z_T| \approx 100 \text{ k}\Omega \quad \text{at low frequency}$$

$$f_{RF-CF} = \frac{1}{2\pi(100 \text{ k}\Omega)(15 \text{ pF})} = 106 \text{ kHz}$$

$$10 \text{ }\mu\text{A} \Rightarrow |V_{OUT}| \approx 1.0 \text{ V}$$

R_F sets the low-frequency current-to-voltage gain. C_F , photodiode junction capacitance and op-amp GBW together determine peaking, bandwidth and stability.

RFspice verification

Download [spice/ACDSPICE_Ch20_Topic04_SPICE.zip](#). A photodiode model with junction capacitance drives a $100 \text{ k}\Omega$ / 15 pF TIA.

Page takeaway

A TIA is a current-interface design: feedback resistance sets conversion gain, while total input capacitance and op-amp dynamics set stability and bandwidth.

20.5. Current-Output Sensors and Shunt Interfaces

Select burden resistance and amplifier gain from the full current range, available compliance voltage and downstream input range.

Current to voltage

A shunt is the simplest current-to-voltage converter: $V_S = I_S R_{SH}$. Its burden voltage is not free; it subtracts from the compliance voltage available to the sensor or loop.

Gain/headroom

Choose the shunt and amplifier gain together. A nominal-point design can clip badly at full-scale current even when every equation is locally correct.

Accuracy

Shunt tolerance and temperature coefficient directly become gain error. High-side measurement adds common-mode constraints and often needs a dedicated current-sense topology.

Key equations

$$V_{SH} = I_S R_{SH}$$

$$P_{SH} = I_S^2 R_{SH}$$

$$A_v = 1 + \frac{R_F}{R_G}$$

$$V_{OUT} = A_v I_S R_{SH}$$

Worked example - why nominal-current design clips

The Topic 05 interface uses a 100 Ohm shunt and a non-inverting stage with $R_F = 40 \text{ k}\Omega$ and $R_G = 10 \text{ k}\Omega$ on $\pm 5 \text{ V}$ rails.

$$V_{SH}(4 \text{ mA}) = (4 \text{ mA})(100 \Omega) = 0.40 \text{ V}$$

$$A_v = 1 + \frac{40k}{10k} = 5$$

$$V_{OUT}(4 \text{ mA}) = 5(0.40) = 2.0 \text{ V}$$

$$V_{OUT}(20 \text{ mA}) = 5(2.0) = 10 \text{ V}$$

The 4 mA point looks valid, but the full-scale 20 mA current would demand 10 V and therefore clips on $\pm 5 \text{ V}$ rails. Shunt value and gain must be selected from the complete current range.

RFspice verification

Download [spice/ACDSPICE_Ch20_Topic05_SPICE.zip](#). The intentionally over-gained 4 mA example shows why full-scale headroom must be checked before committing resistor values.

Page takeaway

Always design a current interface at minimum and maximum current, not just at the nominal point.

20.6. Capacitive Sensors and AC Excitation

Translate capacitance change into an AC amplitude or phase change so tiny capacitive variations can be separated from leakage and DC offset.

Why AC excitation

A static capacitor carries no DC information. Applying an AC carrier makes its impedance $1/(j\omega C)$, so changes in C become measurable changes in divider or bridge voltage.

Bridge approach

A differential capacitive bridge can reject excitation amplitude to first order. Symmetry is valuable because cable capacitance and input capacitance can otherwise dominate the sensor change.

Practical limits

Leakage, dielectric loss, parasitic capacitance, shield/guard capacitance and excitation frequency all matter. Synchronous demodulation is often used after the analog front end.

Key equations

$$Z_C = \frac{1}{j2\pi fC}$$

$$|Z_C| = \frac{1}{2\pi fC}$$

$$V_M = V_{EX} \frac{C_{TOP}}{C_{TOP} + C_{BOTTOM}}$$

$$V_{DIFF} = V_P - V_N$$

Worked example - 100 pF / 105 pF capacitive bridge

The Topic 06 project excites two capacitive divider arms with 1 V AC. One arm is 100 pF / 100 pF; the second uses 100 pF / 105 pF.

$$V_P = 1 \frac{100}{100 + 100} = 0.500 \text{ V}$$

$$V_N = 1 \frac{100}{100 + 105} = 0.4878 \text{ V}$$

$$V_{DIFF} = 0.500 - 0.4878 = 12.2 \text{ mV}$$

$$\frac{\Delta C}{C} = \frac{105 - 100}{100} = 5\%$$

The differential AC output is small compared with the carrier, even for a 5% capacitance change. The 100 MOhm bias paths in the project also show why leakage and parasitics matter at low frequency.

RFspice verification

Download `spice/ACDSPICE_Ch20_Topic06_SPICE.zip`. Change one 100 pF arm to 105 pF and observe the differential AC bridge output.

Page takeaway

Capacitive sensing is usually an AC measurement problem; parasitics are often larger than the signal-producing capacitance change.

20.7. Piezoelectric and Other High-Impedance Sensors

Preserve charge/voltage from high-impedance sensors by controlling input leakage and defining the low-frequency time constant deliberately.

Equivalent source

A piezoelectric element can be represented as generated charge/voltage with a sensor capacitance and leakage. Connecting a finite input resistance creates a high-pass response.

Voltage-mode buffer

A very high input-resistance buffer preserves sensor voltage. The required bias return still determines low-frequency cutoff and makes input bias/leakage important.

Charge amplifiers

For wide sensor capacitance variation or cable capacitance, a charge amplifier can make gain depend mainly on a feedback capacitor rather than on sensor capacitance. That is often preferable for precision piezo measurement.

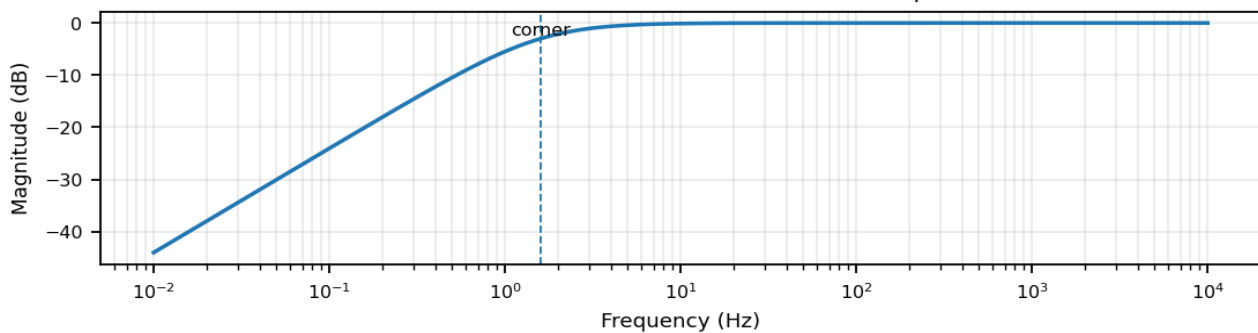
Key equations

$$f_L = \frac{1}{2\pi R_{IN} C_{SENSOR}}$$

$$\tau = R_{IN} C_{SENSOR}$$

$$|H(f)| = \frac{\omega\tau}{\sqrt{1 + (\omega\tau)^2}}$$

Piezo source with 10 nF and 10 MΩ bias path



Worked example - piezo buffer low-frequency corner

The Topic 07 project models a 10 nF high-impedance source with a 10 MΩ bias-return resistor feeding a voltage follower.

$$\tau = (10 \text{ M}\Omega)(10 \text{ nF}) = 0.10 \text{ s}$$

$$f_L = \frac{1}{2\pi(0.10)} = 1.59 \text{ Hz}$$

$$|H(f_L)| = \frac{1}{\sqrt{2}} = 0.707$$

$$20\log_{10}(0.707) = -3.01 \text{ dB}$$

Reducing the bias resistor moves the corner upward and loads the sensor more strongly; increasing it reduces loading but makes input bias current, leakage and contamination more important.

RFspice verification

Download [spice/ACDSPICE_Ch20_Topic07_SPICE.zip](#). A 10 nF source and 10 MΩ bias path feed a high-impedance voltage follower.

Page takeaway

With high-impedance sensors, the bias return resistor and leakage paths become signal-processing components.

20.8. Instrumentation Amplifiers for Bridge Sensors

Build high differential gain without sacrificing input impedance, then protect CMRR by treating resistor ratio accuracy as a first-class specification.

Three-op-amp INA

Two non-inverting input stages provide high input impedance and programmable differential gain. A final difference amplifier rejects common-mode voltage and can add an output reference.

Gain setting

For equal first-stage resistors R and bridge resistor R_G , first-stage differential gain is approximately $1+2R/R_G$. The second-stage resistor ratio multiplies this further.

CMRR reality

The op amps may have excellent intrinsic CMRR, but the difference amplifier resistor ratios can dominate system CMRR. Matched resistor networks are often worth more than tighter absolute resistor values.

Key equations

$$A_{D1} = 1 + \frac{2R}{R_G}$$

$$A_{D2} = \frac{R_F}{R_{IN}}$$

$$A_{TOTAL} = A_{D1}A_{D2}$$

$$V_{OUT} = A_{TOTAL}V_{DIFF}$$

Worked example - three-op-amp INA gain for the bridge

The Topic 08 project uses $R = 10 \text{ k}\Omega$, $R_G = 100 \text{ }\Omega$ in the input pair and a matched $40 \text{ k}\Omega / 10 \text{ k}\Omega$ difference stage.

$$A_{D1} = 1 + \frac{2(10k)}{100} = 201$$

$$A_{D2} = \frac{40k}{10k} = 4$$

$$A_{TOTAL} = 201(4) = 804$$

$$|V_{OUT}| \approx 804(1.25 \text{ mV}) = 1.005 \text{ V}$$

The ideal gain maps the bridge signal to about 1 V. In hardware, resistor ratio matching, amplifier CMRR, input common-mode range and output swing set the real accuracy.

RFspice verification

Download [spice/ACDSPICE_Ch20_Topic08_SPICE.zip](#). A three-op-amp INA amplifies the 1.25 mV bridge signal by about 804 V/V.

Page takeaway

Instrumentation design is about differential gain plus common-mode rejection; resistor ratio matching is part of the amplifier, not a PCB afterthought.

20.9. 4-20 mA Industrial Interfaces, Filtering and Protection

Map a robust current loop into an ADC range while respecting burden voltage, surge paths, cable noise and fault conditions.

Range mapping

A 165 Ohm shunt maps 4-20 mA into approximately 0.66-3.30 V. This uses nearly all of a 3.3 V ADC span but leaves little full-scale margin.

Filtering

A series resistor and capacitor at the receiver can reduce conducted RF/noise and help drive a switched ADC input. Its pole must remain above the wanted sensor bandwidth.

Protection

Input TVS/clamps, series impedance, grounding and isolation requirements depend on cable environment. A small-signal diode in simulation demonstrates current paths but is not a complete surge qualification design.

Key equations

$$V_{SH} = IR_{SH}$$

$$P_{SH} = I^2 R_{SH}$$

$$f_C = \frac{1}{2\pi RC}$$

$$V_{ADC} = IR_{SH}$$

Worked example - map 4-20 mA directly into 0-3.3 V

The Topic 09 receiver uses $R_{SH} = 165 \text{ Ohm}$ followed by a $1 \text{ kOhm} / 1 \text{ uF}$ low-pass.

$$V(4 \text{ mA}) = (4 \text{ mA})(165 \text{ }\Omega) = 0.66 \text{ V}$$

$$V(20 \text{ mA}) = (20 \text{ mA})(165 \text{ }\Omega) = 3.30 \text{ V}$$

$$P_{SH, \max} = (20 \text{ mA})^2 (165 \text{ }\Omega) = 66 \text{ mW}$$

$$f_C = \frac{1}{2\pi(1 \text{ k}\Omega)(1 \text{ }\mu\text{F})} = 159 \text{ Hz}$$

The nominal mapping uses the entire 3.3 V span, so practical hardware needs margin for loop-current tolerance, shunt tolerance, ADC absolute maximum and clamp current.

RFspice verification

Download [spice/ACDSPICE_Ch20_Topic09_SPICE.zip](#). The receiver includes a 165 Ohm shunt, RC filtering and rail clamp paths.

Page takeaway

Industrial interfaces are specified by fault conditions and cable environment as well as nominal transfer gain.

20.10. Worked Design: Bridge Sensor to ADC Range

Combine excitation, differential sensing, gain, level shift, filtering and ADC headroom into one traceable design.

Specification

Use a 5 V, 350 Ohm quarter bridge with GF=2 and +/-500 microstrain range. Map the resulting differential signal around a 1.65 V midpoint so a nominal 0-3.3 V ADC can measure both strain polarities.

Gain budget

The bridge gives about +/-1.25 mV. Gain near 804 produces approximately +/-1.0 V, yielding about 0.65-2.65 V around the 1.65 V reference.

Bandwidth

A final 1.6 kOhm / 100 nF pole is about 995 Hz. That is high enough for many mechanical sensors but low enough to limit broadband noise and ADC kickback. The final value must follow the actual sensor bandwidth and sample rate.

Key equations

$$V_{BRIDGE} \approx \pm 1.25 \text{ mV}$$

$$A_{TOTAL} \approx 804$$

$$V_{ADC} \approx 1.65 \text{ V} \pm 1.0 \text{ V}$$

$$f_{LP} = \frac{1}{2\pi(1.6 \text{ k}\Omega)(100 \text{ nF})} \approx 995 \text{ Hz}$$

Worked example - complete bridge-to-ADC range check

The final design combines the +/-1.25 mV bridge signal, gain about 804, 1.65 V midpoint and a 1.6 kOhm / 100 nF final low-pass.

$$804(1.25 \text{ mV}) = 1.005 \text{ V}$$

$$V_{ADC, min} \approx 1.65 - 1.005 = 0.645 \text{ V}$$

$$V_{ADC, max} \approx 1.65 + 1.005 = 2.655 \text{ V}$$

$$f_{LP} = \frac{1}{2\pi(1.6 \text{ k}\Omega)(100 \text{ nF})} = 995 \text{ Hz}$$

The nominal signal remains inside 0-3.3 V with substantial headroom. The design method on this page then requires excitation, resistor-ratio, temperature, supply and amplifier common-mode/output-swing corners.

Design method

- Verify bridge common-mode and differential range.
- Check amplifier input common-mode and output swing.
- Include reference tolerance and resistor ratio error.
- Set analog bandwidth from the physical sensor and ADC sample rate.
- Run min/max excitation, strain, temperature and supply corners.

RFspice verification

Download [spice/ACDSPICE_Ch20_Topic10_SPICE.zip](#). The functional complete chain maps the bridge into the ADC range; replace the gain block with the Topic 08 INA for transistor/op-amp implementation.

Page takeaway

A sensor front end is complete only when physical range, electrical source model, common mode, gain, offset, bandwidth and ADC limits are all checked together.