

11.1. Why Variable Gain and AGC are Different from Fixed Gain

Define the controlled quantity, gain range and loop objective before choosing a circuit.

Variable gain amplifier

A VGA provides gain A that is intentionally controlled by a voltage or current. The control may be manual, digitally generated or produced by an automatic loop.

Automatic gain control

AGC measures some representation of output amplitude, compares it with a target and adjusts the VGA. The complete system therefore contains a signal path and a much slower control path.

Specifications

Important numbers include minimum/maximum gain, gain-control law, input/output dynamic range, distortion, noise, bandwidth, detector accuracy, attack time, release time and residual level error.

Specification	Circuit consequence
Wide gain range	control device must remain monotonic over decades of signal level
Low distortion	gain element must stay in its linear region
Fast attack	detector/control bandwidth must be high enough
Low ripple/pumping	control bandwidth must be well below signal/envelope variations

Key equations

$$G_{dB} = 20 \log_{10} \left| \frac{V_{out}}{V_{in}} \right|$$

$$\Delta G_{dB} = G_{max, dB} - G_{min, dB}$$

$$A_{req} = \frac{V_{target}}{V_{in}}$$

$$\text{AGC: } V_{out} \rightarrow \text{detector} \rightarrow \text{error/filter} \rightarrow \text{gain control}$$

Worked example - turn an input dynamic range into a required gain range

Suppose an AGC must hold the output near 0.50 Vpk while the input may vary from 5 mVpk to 0.50 Vpk.

$$A_{max} = \frac{0.50}{0.005} = 100 \Rightarrow G_{max} = 40 \text{ dB}$$

$$A_{min} = \frac{0.50}{0.50} = 1 \Rightarrow G_{min} = 0 \text{ dB}$$

$$\Delta G = 40 - 0 = 40 \text{ dB}$$

$$\text{required linear gain ratio} = 10^{40/20} = 100 : 1$$

This 40 dB requirement belongs to the VGA. Attack/release time, detector accuracy and loop stability are separate AGC requirements and should not be hidden inside the gain-range number.

Page takeaway

AGC is a feedback system around a variable-gain circuit. Design the VGA and the control loop as separate problems first.

11.2. Gain Control by Degeneration

Start with the simplest controllable quantity: effective emitter/source degeneration.

Gain equation

For a degenerated transistor stage, midband gain is approximately the collector/drain load divided by the sum of intrinsic emitter/source resistance and explicit degeneration.

Electronic implementation

A switched resistor bank gives discrete gain. A FET operated as a voltage-controlled resistance can provide continuous control, but its resistance is signal-dependent and therefore creates distortion if too much signal appears across it.

Design lesson

Before choosing an electronic control element, establish how much degeneration change is required to achieve the specified gain range. That defines the resistance-control range and linearity burden.

Key equations

$$A_v \approx -\frac{R_C \parallel R_L}{r_e + R_E}$$

$$r_e \approx \frac{V_T}{I_E}$$

$$R_E \uparrow \Rightarrow |A_v| \downarrow$$

$$\text{control ratio} \approx \frac{r_e + R_{E,max}}{r_e + R_{E,min}}$$

Worked example - compare three degeneration settings

Use $R_C = 2.2 \text{ k}\Omega$, $R_L = 47 \text{ k}\Omega$, so the AC collector load is about $2.10 \text{ k}\Omega$. For a clean comparison assume $I_E = 2 \text{ mA}$, giving r_e about $12.9 \text{ }\Omega$.

$$R_C \parallel R_L = 2.2 \text{ k}\Omega \parallel 47 \text{ k}\Omega = 2.10 \text{ k}\Omega$$

$$R_E = 100 \text{ }\Omega: \quad A_v \approx -\frac{2.10 \text{ k}\Omega}{112.9 \text{ }\Omega} = -18.6$$

$$R_E = 470 \text{ }\Omega: \quad A_v \approx -4.35$$

$$R_E = 1.0 \text{ k}\Omega: \quad A_v \approx -2.07$$

This isolates the gain-control mechanism. In the actual Topic 02 circuits, changing R_E also shifts the DC operating point, so RFspice .op results should be used to recalculate r_e before comparing measured AC gain.

RFspice verification

Download `spice/ACDSPICE_Ch11_Topic02_SPICE.zip`. Three otherwise identical BJT stages show how 100, 470 and 1000 Ω of degeneration change gain.

Page takeaway

Variable degeneration is intuitive and robust, but the control element itself must be linear enough for the signal amplitude it sees.

11.3. Tail Current as a Transconductance Control

Use the differential pair itself as a current-programmed gain element.

The key relationship

For a balanced BJT pair, each transistor current is $I_T/2$, giving $g_m = I_T/(2V_T)$. If the collector load is fixed, differential voltage gain is approximately proportional to tail current.

Control range and headroom

Increasing I_T increases gain but also increases voltage drop in collector loads and device dissipation. The usable control range ends when headroom is lost or when beta, Early effect and high-current g_m compression invalidate the simple model.

Noise trade-off

Lower current reduces g_m and gain but can worsen input-referred voltage noise. AGC therefore changes not just gain but sometimes noise figure and bandwidth.

Key equations

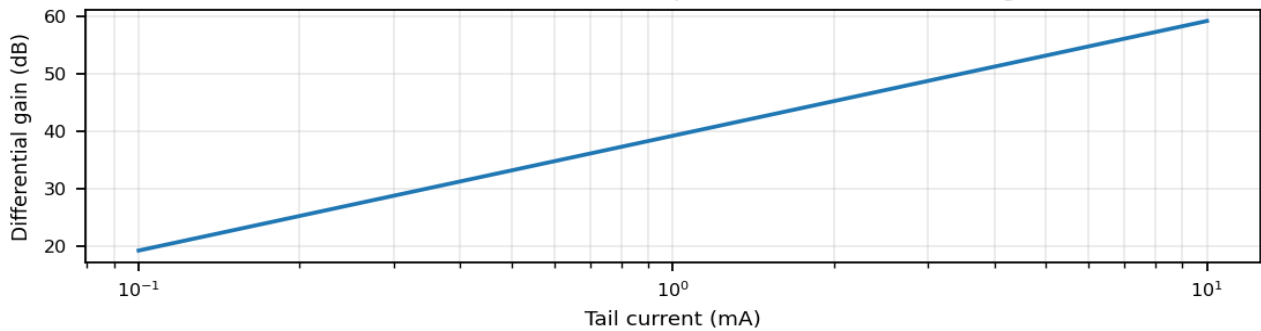
$$g_m = \frac{I_T}{2V_T}$$

$$A_{d,diff} \approx -\frac{I_T}{2V_T} R_{load}$$

$$\frac{A_{v2}}{A_{v1}} \approx \frac{I_{T2}}{I_{T1}} \quad \text{while headroom permits}$$

$$I_T \uparrow \Rightarrow g_m \uparrow \Rightarrow |A_v| \uparrow$$

tail current controls differential-pair transconductance and gain



Worked example - calculate gain from programmed tail current

Topic 03 uses $R_C = 4.7 \text{ k}\Omega$ and tail currents of 0.2, 1 and 2 mA. Ignore r_o for the first pass.

$$I_T = 0.2 \text{ mA}: \quad g_m = \frac{0.2 \text{ mA}}{2(25.85 \text{ mV})} = 3.87 \text{ mS}, \quad |A_d| = 18.2$$

$$I_T = 1.0 \text{ mA}: \quad g_m = 19.3 \text{ mS}, \quad |A_d| = 90.9$$

$$I_T = 2.0 \text{ mA}: \quad g_m = 38.7 \text{ mS}, \quad |A_d| = 181.9$$

$$\frac{|A_d(2 \text{ mA})|}{|A_d(0.2 \text{ mA})|} \approx 10$$

The gain tracks tail current almost directly until collector headroom, finite r_o and high-current device effects intervene. This is the physical basis of a transconductance-controlled VGA.

RFspice verification

Download [spice/ACDSPICE_Ch11_Topic03_SPICE.zip](#). Compare 0.2, 1 and 2 mA tail currents with identical differential pairs.

Page takeaway

Tail-current control is a direct way to turn bias current into gain control because the controlled physical quantity is g_m .

11.4. Differential Current Steering and the Gilbert Gain Cell

Separate signal conversion from gain control using stacked differential pairs.

Two differential operations

A lower pair converts input voltage to differential current. An upper transistor quad then steers that current between output nodes according to a second differential control voltage.

Multiplication viewpoint

For small signal and control voltages the circuit behaves approximately as a multiplier: output is proportional to signal times a function of control voltage. Larger control voltages progressively steer nearly all current to one side.

Practical limits

Every stacked transistor consumes headroom. Matching affects feedthrough and offset. The signal pair must remain in its linear range, and the control pair must be biased so the gain law is monotonic over the required range.

Key equations

$$i_{sig} \approx g_m v_{sig}$$

$$s(v_c) = \tanh\left(\frac{v_c}{2V_T}\right)$$

$$i_{out} \approx i_{sig} s(v_c)$$

$$v_{out} \propto v_{sig} \tanh\left(\frac{v_c}{2V_T}\right)$$

Worked example - evaluate the Gilbert steering control factor

For the Topic 04 current-steering cell, use $V_T = 25.85$ mV. The signal pair has roughly 0.5 mA per device, so g_m is about 19.3 mS and the collector resistors are 3.3 kOhm.

$$v_c = 25 \text{ mV} : \quad s = \tanh\left(\frac{25}{51.7}\right) = 0.449$$

$$v_c = 75 \text{ mV} : \quad s = \tanh\left(\frac{75}{51.7}\right) = 0.896$$

$$g_m R_C \approx (19.3 \text{ mS})(3.3 \text{ k}\Omega) = 63.7$$

$|A_v|$ scales roughly from 0 at $v_c = 0$ to 28.6 and 57.1 V/V

The exact circuit is a stacked transistor network, so headroom and output loading modify these values. The calculation shows why tens of millivolts of control voltage can sweep a BJT steering cell across most of its gain range.

Deeper engineering point

The Gilbert structure is powerful because control is differential and largely isolated from the signal input, but it costs voltage headroom and demands matching.

RFspice verification

Download [spice/ACDSPICE_Ch11_Topic04_SPICE.zip](#). The six-BJT current-steering cell changes signal transfer as the control voltage steps.

Page takeaway

Current steering turns the differential pair from a fixed- g_m amplifier into the foundation of VGAs, multipliers and mixers.

11.5. Gain-Control Law: Linear Gain versus dB-Linear Gain

Choose the control law to match the system dynamic range and controller.

Linear control

If $A=A_0+kV_c$, equal control-voltage steps create equal changes in linear gain. This is convenient over a modest range but awkward when gain must span decades.

dB-linear control

If gain is exponential in control voltage, GdB becomes approximately linear with control voltage. Many RF/IF VGAs are specified in dB/V because AGC dynamic range is naturally expressed in decibels.

Characterise before closing the loop

Measure or simulate gain versus control voltage, signal frequency, temperature and amplitude. The controller can only regulate predictably over the monotonic, usable part of that surface.

Key equations

$$A(V_c) = A_0 + kV_c \quad \text{linear gain law}$$

$$A(V_c) = A_0 e^{kV_c} \quad \text{exponential law}$$

$$G_{dB} = 20 \log_{10} A$$

$$\text{exponential law : } \frac{dG_{dB}}{dV_c} = 20 \log_{10}(e) k \approx 8.686k$$

Worked example - translate control voltage into gain and dB

Topic 05 deliberately uses the transparent behavioural law $A = 0.2 + 9.8V_c$. Evaluate the three control levels used in the transient test.

$$V_c = 0 : \quad A = 0.20, \quad G = 20 \log_{10}(0.20) = -14.0 \text{ dB}$$

$$V_c = 0.25 : \quad A = 2.65, \quad G = 8.46 \text{ dB}$$

$$V_c = 0.75 : \quad A = 7.55, \quad G = 17.6 \text{ dB}$$

$$100 \text{ mV}_{pk} \text{ input} \Rightarrow 0.020, 0.265, 0.755 \text{ V}_{pk} \text{ outputs}$$

This example is linear in gain, not linear in dB. An exponential control law is preferred when equal control-voltage increments must correspond to equal dB increments over a wide dynamic range.

RFspice verification

Download [spice/ACDSPICE_Ch11_Topic05_SPICE.zip](#). A transparent behavioural VGA makes the control-law concept measurable without transistor complications.

Page takeaway

The gain-control curve is part of the plant. AGC design needs its slope and limits, not merely its maximum gain.

11.6. Amplitude Detection and Envelope Filtering

Convert an AC output into the slowly varying quantity that the control loop can compare with a reference.

Diode detector

A diode and capacitor provide a simple peak/envelope detector. The capacitor charges near peaks and discharges through a resistor between them. Diode drop, source resistance and loading create amplitude error.

Ripple versus response speed

A large RC time constant gives low ripple but slow response to changing level. A small time constant follows level quickly but passes more carrier/envelope ripple into the gain-control path.

Other detectors

Precision rectifiers reduce diode-drop error. RMS detectors regulate signal power rather than peak amplitude. Log detectors provide large dynamic range and can naturally support dB-domain control.

Key equations

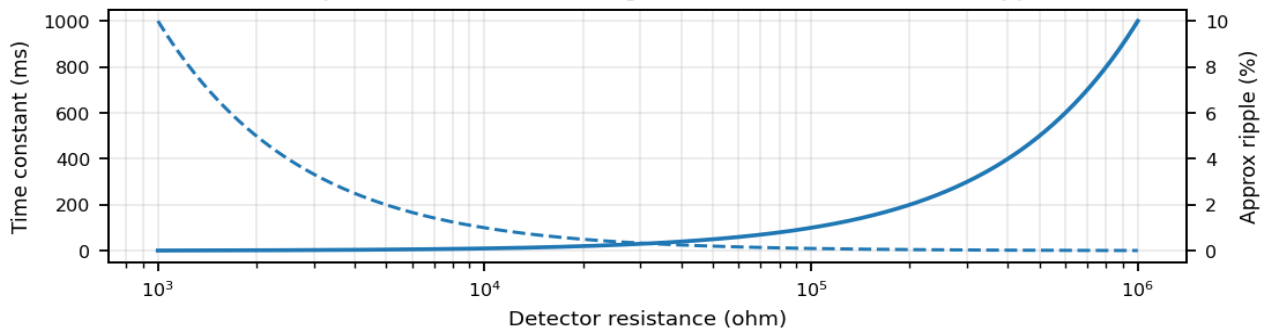
$$\tau_{det} = R_{det}C_{det}$$

$$T_s = \frac{1}{f_s}$$

$$\tau_{det} \gg T_s \text{ for low carrier ripple}$$

$$\text{ripple roughly falls as } T_s/\tau_{det} \text{ when } \tau_{det} \gg T_s$$

Envelope detector trade-off: longer time constant means less ripple



Worked example - quantify detector ripple versus response time

Topic 06 uses $R_{det} = 22 \text{ k}\Omega$, $C_{det} = 1 \text{ }\mu\text{F}$ and a 10 kHz input.

$$\tau = (22 \text{ k}\Omega)(1 \text{ }\mu\text{F}) = 22 \text{ ms}$$

$$T_s = \frac{1}{10 \text{ kHz}} = 100 \text{ }\mu\text{s}$$

$$\frac{\tau}{T_s} = \frac{22 \text{ ms}}{100 \text{ }\mu\text{s}} = 220$$

$$\frac{T_s}{\tau} \approx 0.00455 \Rightarrow \text{only about 0.46\% decay per cycle for small ripple}$$

A 22 ms detector is smooth compared with a 100 us carrier period, but it is also slow to follow amplitude changes. The diode forward drop adds a separate amplitude error that the RC calculation does not remove.

RFspice verification

Download [spice/ACDSPICE_Ch11_Topic06_SPICE.zip](#). A 10 kHz diode detector with 22 kOhm and 1 uF shows the basic envelope/ripple compromise.

Page takeaway

The detector defines what the AGC actually regulates: peak, average, RMS or log amplitude are not interchangeable.

11.7. Reference, Error Amplifier and Correct Loop Polarity

Make sure a larger-than-target output always commands less gain.

Error definition

A convenient error is $e = V_{ref} - V_{det}$. If the output is too small, V_{det} is below V_{ref} and the control circuit should increase gain. If the output is too large, control should reduce gain.

Controller gain

More control gain reduces static level error but can cause overshoot or hunting once detector/filter delay is included. The AGC loop is a low-frequency feedback loop even when the signal path operates at much higher frequency.

Saturation and wind-up

The VGA has minimum and maximum gain. The controller output should be limited to that usable control range. Otherwise the control node can rail and recovery from overload may be unnecessarily slow.

Key equations

$$e = V_{ref} - V_{det}$$

$$V_{control} = K_e e$$

$$V_{det} \uparrow \Rightarrow V_{control} \downarrow \Rightarrow \text{gain} \downarrow$$

controller output must remain inside the usable VGA control range

Worked example - check the AGC polarity numerically

Topic 07 sets $V_{ref} = 1.0 \text{ V}$ and uses $V_{control} = 2(V_{ref} - V_{det})$. Evaluate detector values below, at and above target.

$$V_{det} = 0.60 \text{ V} : \quad V_c = 2(1.0 - 0.60) = +0.80 \text{ V}$$

$$V_{det} = 1.00 \text{ V} : \quad V_c = 0$$

$$V_{det} = 1.40 \text{ V} : \quad V_c = 2(1.0 - 1.40) = -0.80 \text{ V}$$

$V_{det} \uparrow \Rightarrow V_c \downarrow$ so the following VGA must map lower V_c to lower gain

This sign test should be performed through the complete control chain. If any later block inverts the command unexpectedly, the loop becomes positive feedback and drives to a rail.

RFspice verification

Download [spice/ACDSPICE_Ch11_Topic07_SPICE.zip](#). Sweep detector voltage around a 1 V reference and verify the control-polarity sign before closing a loop.

Page takeaway

A one-minute polarity test prevents the most destructive AGC mistake: accidentally making the amplitude loop positive feedback.

11.8. Attack, Release and Gain Pumping

Design different control time constants for overload protection and smooth recovery.

Attack

Attack time determines how quickly gain reduces after a sudden input increase. If it is too slow, the signal path clips before the loop reacts.

Release

Release time determines how quickly gain rises after input level falls. A slower release often prevents the gain from audibly or visibly following individual waveform envelopes.

Asymmetric networks

Oppositely oriented diodes can provide separate charging and discharging resistances around one control capacitor. The control filter is therefore nonlinear, but intentionally so.

Key equations

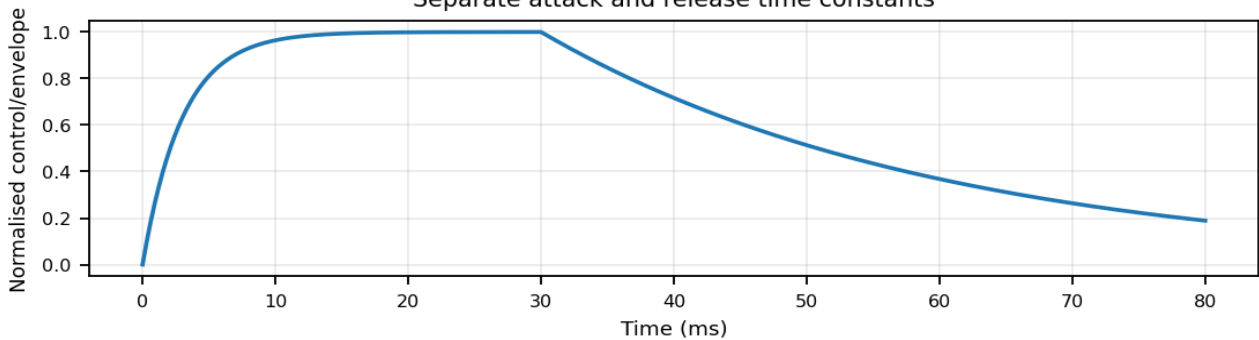
$$\tau_{\text{attack}} \approx R_{\text{attack}} C_{\text{control}}$$

$$\tau_{\text{release}} \approx R_{\text{release}} C_{\text{control}}$$

$$t_{63\%} = \tau, \quad t_{95\%} \approx 3\tau$$

$$\tau_{\text{release}} \gg \tau_{\text{attack}} \text{ is common when pumping must be reduced}$$

Separate attack and release time constants



Worked example - calculate asymmetric attack and release times

Topic 08 uses $C_{\text{control}} = 1 \mu\text{F}$, $R_{\text{attack}} = 2.2 \text{ k}\Omega$ and $R_{\text{release}} = 47 \text{ k}\Omega$.

$$\tau_{\text{attack}} = (2.2 \text{ k}\Omega)(1 \mu\text{F}) = 2.2 \text{ ms}$$

$$\tau_{\text{release}} = (47 \text{ k}\Omega)(1 \mu\text{F}) = 47 \text{ ms}$$

$$t_{95\%, \text{attack}} \approx 3\tau = 6.6 \text{ ms}$$

$$t_{95\%, \text{release}} \approx 3\tau = 141 \text{ ms}$$

Release is about 21 times slower than attack. That lets the AGC reduce gain quickly during an overload while restoring gain gently enough to reduce visible or audible pumping.

RFspice verification

Download [spice/ACDSPICE_Ch11_Topic08_SPICE.zip](#). A diode-separated $2.2 \text{ k}\Omega$ attack path and $47 \text{ k}\Omega$ release path drive a $1 \mu\text{F}$ control capacitor.

Page takeaway

Attack protects headroom; release controls subjective smoothness and pumping. There is rarely one optimum time constant for both.

11.9. AGC Loop Dynamics, Stability and Practical Limits

Treat the detector, control filter and VGA slope as a feedback loop with finite bandwidth.

Loop gain

The effective low-frequency loop gain is the product of detector slope, controller gain and VGA gain-control slope. Higher loop gain improves regulation until phase lag and delay cause ringing or hunting.

Bandwidth separation

The control loop should normally be much slower than the carrier/signal cycles it is measuring, yet fast enough for the required level changes. Detector ripple that reaches the VGA becomes amplitude modulation.

Limits outside the loop

AGC cannot repair clipping that occurs before the controlled gain element. Noise may be amplified at maximum gain. At minimum gain the stage still needs enough linear range for the largest specified input.

Key equations

$$T_{loop}(s) \approx K_{det} K_{ctrl}(s) \frac{dA}{dV_c}$$

regulation error $\propto \frac{1}{1+|T_{loop}|}$ at low frequency

$$\tau_{det} = R_{det} C_{det}$$

control bandwidth $\ll$ signal frequency but must follow required envelope changes

Worked example - inspect the behavioural AGC operating law

Topic 09 has a 10 kOhm/2 uF detector and controller GAIN = clamp[1 + 12(0.5 - ENV), 0.2, 12].

$$\tau_{det} = (10 \text{ k}\Omega)(2 \text{ }\mu\text{F}) = 20 \text{ ms}$$

$$ENV = 0.20 \text{ V: } GAIN = 1 + 12(0.30) = 4.6$$

$$ENV = 0.50 \text{ V: } GAIN = 1.0$$

$$ENV = 0.60 \text{ V: } GAIN = 1 + 12(-0.10) = -0.2 \Rightarrow \text{clamped to } 0.2$$

The detector is intentionally slow compared with the 10 kHz carrier. The control slope is strong, so the clamp matters: without it, large errors would command impossible negative or excessive gain.

Deeper engineering point

Do not increase AGC loop gain simply because the output-level error seems too large. First identify detector lag, VGA control slope and any hard gain limits.

RFspice verification

Download spice/ACDSPICE_Ch11_Topic09_SPICE.zip. A behavioural AGC loop applies a fourfold input-amplitude step so detector time constant and controller gain can be explored safely.

Page takeaway

AGC dynamics are feedback dynamics: gain, delay, poles, saturation and disturbance bandwidth all matter.

11.10. Worked Design: Differential AGC Amplifier

Close an amplitude-control loop around a transistor differential pair whose g_m is programmed by tail current.

Architecture

A BJT differential pair drives two collector resistors. A controlled tail-current sink changes g_m and therefore differential gain. A differential-output block feeds an amplitude detector, RC filter and error controller.

Design target

The teaching design accepts an input that steps from 20 mVpk to 100 mVpk at 10 kHz. The control loop attempts to keep the detected differential output near a 0.45 V reference while constraining tail current to 0.05-2 mA.

Why a behavioural controller is used

The signal gain cell is transistor-level so g_m , headroom and distortion are real. The detector/controller is deliberately transparent so students can see the loop law before replacing it with precision rectifiers, op-amps or log-detector ICs.

Verification

Plot input, differential output, detected envelope, control voltage and tail current. Confirm correct loop polarity, no rail clipping, bounded tail current and a sensible attack time. Then change detector RC and controller slope one at a time.

Key equations

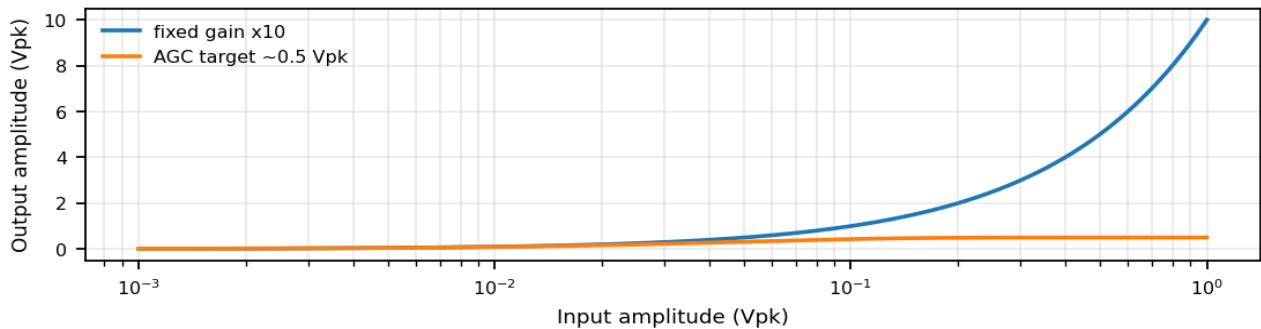
$$I_T = \text{clamp}(I_{\min} + K_I V_C, I_{\min}, I_{\max})$$

$$g_m = \frac{I_T}{2V_T}$$

$$V_C = \text{clamp}(V_{C0} + K_e(V_{\text{ref}} - V_{\text{env}}), 0, 1)$$

$$A_{d,\text{diff}} \approx -g_m R_C \text{ before } r_o \text{ and headroom corrections}$$

Closed-loop AGC compresses a wide input range toward a target level



Worked example - map envelope error into tail current and gain

Topic 10 uses $\text{CTRL} = \text{clamp}[0.5 + 2(0.45 - \text{ENV}), 0, 1]$ and $I_T = 50 \mu\text{A} + 1.95 \text{ mA} \cdot \text{CTRL}$, with 3.3 kOhm collector resistors.

$$\text{ENV} = 0.45 \text{ V: } \text{CTRL} = 0.50, \quad I_T = 1.025 \text{ mA}$$

$$g_m = \frac{1.025 \text{ mA}}{2(25.85 \text{ mV})} = 19.8 \text{ mS}, \quad |A_d| \approx 65.4$$

$$\text{ENV} = 0.60 \text{ V: } \text{CTRL} = 0.20, \quad I_T = 0.440 \text{ mA}, \quad |A_d| \approx 28.1$$

$$\text{ENV} = 0.20 \text{ V: } \text{CTRL} \rightarrow 1, \quad I_T \rightarrow 2.00 \text{ mA}, \quad |A_d| \approx 127.7$$

As the detected output rises above target, the loop reduces CTRL, tail current and g_m . The gain cell is transistor-level, so the final transient must also be checked for collector clipping and the specified 0.05-2 mA tail-current limits.

Design method

- Verify the VGA open-loop gain range first.
- Verify detector scaling and ripple independently.
- Verify loop polarity with a forced detector voltage.
- Close the loop at modest controller gain.
- Increase speed only while transient response remains well damped.
- Test minimum and maximum input amplitudes and confirm no earlier stage clips.

RFspice verification

Download [spice/ACDSPICE_Ch11_Topic10_SPICE.zip](#). The complete RFspice project exposes every AGC state variable for transient inspection.

Page takeaway

A differential AGC is a synthesis of device physics, small-signal gain, nonlinear detection and feedback. Design each block separately, then close and verify the loop.